Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A semiconductor memory device having a plurality of memory cells arranged in an array, comprising:

a flip-flop of said memory cells having a pair of inverters formed of driver MOS (Metal Oxide Semiconductor) transistors and load elements;

a pair of access MOS transistors of said memory cells electrically connected to input nodes of said inverters respectively;

an interlayer insulation film covering said access MOS transistors and said driver MOS transistors;

a pair of capacitive elements of said memory cells formed on said interlayer insulation film and electrically connected to said input nodes of said inverters;

a word line electrically connected to gate electrodes of said pair of access MOS transistors and extending in the same direction as an extending direction of gate electrodes of said driver MOS transistors and disposed between said gate electrodes of said driver MOS transistors;

a pair of active region patterns formed by integrating a pair of active regions of said access MOS transistors with a pair of active regions of said driver MOS transistors and extending in a direction orthogonal to an extending direction of said word line; and

a pair of bit lines extending in a direction orthogonal to the extending direction of said word line and electrically connected to active regions of said access MOS transistors respectively; wherein

a length of said memory cells in the extending direction of said word line is longer than that in an extending direction of said bit lines,

said bit lines are disposed above said access MOS transistors and said driver MOS transistors,

said load elements are disposed above said bit lines, and

said capacitive elements are disposed above said load elements.

2. (Original) The semiconductor memory device according to claim 1, wherein

a gate width of said driver MOS transistor is at least 0.8 times and at most 1.2 times as large as a gate width of said access MOS transistor.

3. (Original) The semiconductor memory device according to claim 1, wherein

the gate electrode of one of said driver MOS transistors of one of said memory cells and the gate electrode of one of said driver MOS transistors of another memory cell, which is adjacent to said one of memory cells in the extending direction of said word line, are disposed on opposite sides of said active regions of said access MOS transistors which is electrically connected to said bit lines,

the gate electrode of said one of driver MOS transistors of said another memory cell extends into said memory cell.

4. (Original) The semiconductor memory device according to claim 2, further comprising

a pair of ground line, wherein

said pair of bit lines is arranged between said ground lines, and said ground lines are extended in the same direction as said bit lines.

5. (Original) The semiconductor memory device according to claim 1, wherein

said load elements include a thin film transistor respectively,

said thin film transistor includes a first conductive layer functioning as a gate electrode, and a second conductive layer including a source region, a channel region and a drain region,

said first conductive layer is in a substantially triangular shape, and

said second conductive layer is in a curved shape.

6. (Original) The semiconductor memory device according to claim 1, wherein

said load elements include a thin film transistor respectively,

said capacitive elements have first and second electrodes opposing to each other with an insulation film therebetween respectively, and

said first electrode functions as a gate electrode of said thin film transistor.

7. (Original) The semiconductor memory device according to claim 1, wherein

said load elements include a thin film transistor respectively, and

a gate electrode of said thin film transistor and said capacitive element are of the same shape.

8. (Original) The semiconductor memory device according to claim 1, wherein

ratio of parasitic capacitance of said bit line to capacitance of said memory cell is at most 8.

9. (Original) The semiconductor memory device according to claim 1, wherein

resistance value of a contact part of said bit line and said access MOS transistor is set larger than resistance value of a contact part of said driver MOS transistor and said ground line.

10. (Currently Amended) The semiconductor memory device according to claim 1, wherein

the capacitance of said capacitive elements is at least [[10pF]] 10fF and at most [[30pF]] 30fF.